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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/990,739	11/16/2001	David H. Harris	5087-27	3310
20575	7590	07/24/2006	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			DANG, KHANH	
			ART UNIT	PAPER NUMBER
			2111	

DATE MAILED: 07/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/990,739		HARRIS ET AL.	
	Examiner		Art Unit	
	Khanh Dang		2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

In the Final Office Action dated 10/28/2004, claims 1-20 were rejected under 35 USC 102(e) as being anticipated by Jacobs. Specifically, the Examiner maintained the rejection because the Applicants' 37 CFR 1.131 Affidavit filed 8/16/2004 failed to overcome the prior art (Jacobs).

Applicants subsequently filed an Appeal Brief dated 7/1/2005 to argue against the Examiner's position regarding the validity of the 37 CFR 1.131 Affidavit, and to maintain that Jacobs was not appropriately considered as prior art because Applicant's date of invention was prior to the September 27, 2000 filing date of Jacobs.

Upon reviewing Applicants' Appeal Brief and 131 Affidavit, it is now determined that Applicants are entitled to the benefit of the doubts, and therefore, the 131 Affidavit is considered valid, and thus, overcomes the Jacobs 102 Rejection.

The 10/28/2004 Final Rejection over Jacobs is hereby withdrawn.

A new ground of rejection is set forth below:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi (6,199,122).

As broadly drafted, these claims do not define any structure/step that differs from Kobayashi.

With regard to claim 1, Kobayashi discloses a method of communicating with a mass storage device, comprising: receiving ATA/ATAPI signals from a mass storage device into a bridging circuit (in Kobayashi, ATA signals from the memory device 13 of the storage device 12, for example, are received by a single chip conversion controller 122, for example, or the so-called "bridging circuit"; see at least column 1, lines 1-22, column 5, lines 56-58, and column 6, lines 12-13; note also that ATA standard in Kobayashi includes ATA/ATAPI, see definition of ATA from Wikipedia cited below); converting the ATA/ATAPI signals from the mass storage device into USB signals using the bridging circuit (in Kobayashi, the ATA signals from the memory device 13 of the storage device 12 is converted into USB signals by the single chip conversion controller 122; see at least column 6, lines 1-22, and column 12, lines 33-39) ; and outputting the USB signals from the bridging circuit (in Kobayashi, USB signals are outputted from the conversion controller 122; see at least column 6, lines 1-22, and column 12, lines 33-39).

With regard to claim 2, it is clear that the conversion controller is provided in a single chip; see at least column 6, lines 12-13.

With regard to claim 3, it is clear from at least Fig. 1, and at least column 6, lines 12-13, that the conversion controller is a single chip. Thus, the conversion controller single chip 122 must be provided on a motherboard of the mass storage device 12 (column 5, lines 56-58).

With regard to claim 4, since claim 1 is so broadly drafted, the motherboard of the storage device 12 having memory device 13 connected thereto is in fact, can be considered as a "secondary board." Note that the computer clearly includes another motherboard or mainboard.

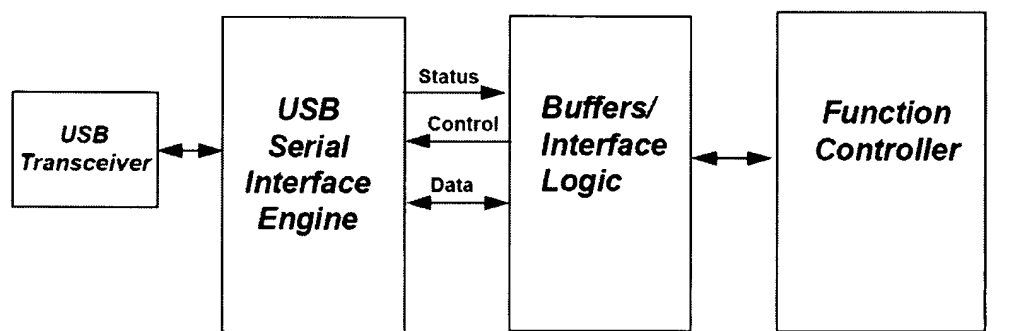
With regard to claim 6, see discussion above, since the subject matter presented in claim 6 has already been discussed. Note that Kobayashi further discloses that "the ATA controller 124 is a read/write controller based on the ATA standard and reads/writes data from and into the memory card 13." Note also that it is clear that the external storage device 12 must include a motherboard so that IC components such as the conversion controller 122 can be attached thereto.

With regard to claim 7, see discussion above, since the subject matter presented in claim 7 has already been discussed.

With regard to claim 8, see discussion above, since the subject matter presented in claim 8 has already been discussed. Note that it is clear from discussion above that the single chip conversion controller 122 is used to convert ATA/ATAPI signals to USB signals and vice versa. Thus, it is clear that the single chip conversion controller 122 includes an ATA/ATAPI interface to take the ATA/ATAPI signal and convert it to a USB signal, a disk interface (any ATA standard provides disk interface) and also a USB

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interface. Further, since the single chip conversion controller 122 also employs USB protocol for sending USB signals to computer 111 having a USB interface, it must be in full compliance with the USB specification, which requires a serial interface engine; and a USB physical interface transceiver configured to receive signals from the serial interface engine and output USB signals to a USB interface. The following is a diagram of a USB hardware interface according to the USB specification. See designing a robust USB Serial Interface Engine, cited below.



With regard to claims 13-15, see discussion above, since the subject matter presented in claim 13 has already been addressed.

With regard to claim 16, since claims 13-15 are so broadly drafted, the motherboard of the storage device 12 having memory device 13 connected thereto is in fact, can be considered as a “secondary board.” Note that the computer clearly includes another motherboard.

With regard to claims 18-19, see discussion above, since the subject matter presented in claims 18-19 has already been addressed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 17, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi.

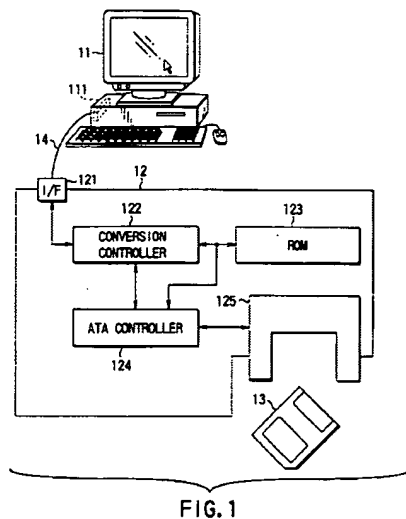
Kobayashi, as discussed above, discloses the claimed invention including the use of a single chip conversion controller 122 or the so-called "bridge circuit."

Kobayashi does not disclose that the single chip conversion controller 122 is provided on a secondary board, wherein a mass storage device motherboard outputs ATA/ATAPI signals, and wherein the secondary board receives the ATA/ATAPI signals from the mass storage device motherboard and converts them into USB signals.

In other words, the difference between the claimed subject matter and that of Kobayashi resides on the fact that the in Kobayashi, the single chip conversion controller 122 resides on the motherboard of the storage device 12, whereas in the instant application, the conversion controller or "bridge circuit" (as claimed in claim 5) is provided on a separate or "secondary" board.

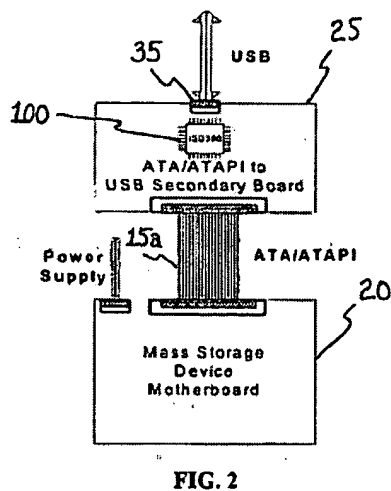
Such a difference is best illustrated by the following figures:

Fig. 1 of Kobayashi:



Note that the single chip conversion controller 122 or the so-called "bridge circuit" is provided on the motherboard of the storage device 12.

Fig. 2 of the instant Application:



Note that the so-called "bridge circuit" (single chip) 100 is provided on a separate "secondary" board 25, instead of on the motherboard 20 of the storage device.

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However, it is clear that whether the single chip conversion controller 122 or the so-called "bridge circuit" is provided on the motherboard of the storage device as in Kobayashi, or provided on a separate or "secondary" board as in claim 5, the conversion controller 122 would perform the same function, which is a function of converting between the ATA/ATAPI protocol to the USB protocol and vice versa. As matter of fact, as disclosed in Applicants' summary of the Invention, the crux of Applicants' claimed invention is a single bridging chip for converting ATA/ATAPI protocol to USB protocol and vice versa. The bridging circuit/chip 100 would perform the same function whether the bridging chip 100 is provided on a motherboard of the storage device (page 2, lines 8-12 of the originally filed specification, and Fig. 3):

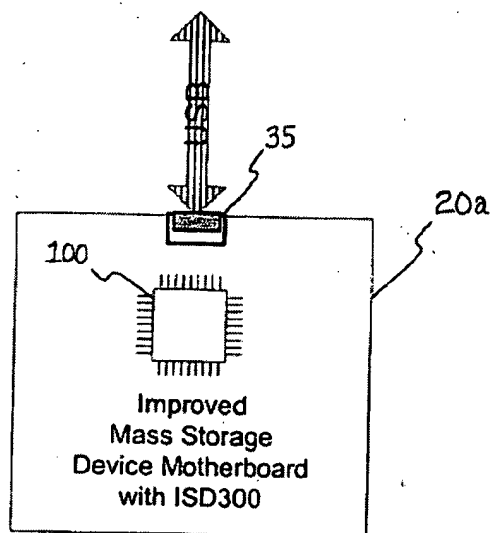


FIG. 3

or, **alternatively**, as a design choice, the bridging chip 100 is provided on a secondary board (see page 2, lines 17-21 of the originally filed specification, and Fig. 2)

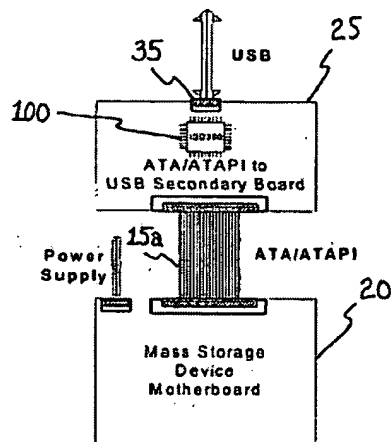


FIG. 2

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a separate or "secondary" board for the single chip conversion controller 122 of Kobayashi, since the conversion controller chip 122 of Kobayashi would perform the same function whether on the same board with the storage device 12 or on a separate or "secondary board" and, thus, providing a separate or "secondary board" for the single chip conversion controller 122 of Kobayashi is a matter of design choice, as also acknowledged by Applicants, and only involves ordinary skill in the art.

Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi.

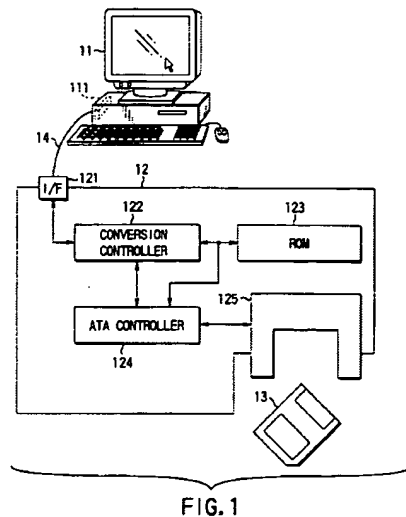
Kobayashi, as discussed above, discloses the claimed invention including the use of a single chip conversion controller 122 or the so-called "bridge circuit."

Kobayashi does not disclose that the single chip conversion controller 122 is provided on a secondary board, wherein a mass storage device motherboard outputs ATA/ATAPI signals, and wherein the secondary board receives the ATA/ATAPI signals from the mass storage device motherboard and converts them into USB signals.

In other words, the difference between the claimed subject matter and that of Kobayashi resides on the fact that the in Kobayashi, the single chip conversion controller 122 resides on the motherboard of the storage device 12, whereas in the instant application, the conversion controller or "bridge circuit" (as claimed in claim 5) is provided on a separate or "secondary" board.

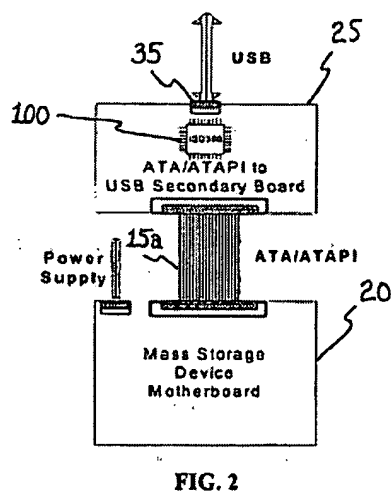
Such a difference is best illustrated by the following figures:

Fig. 1 of Kobayashi:



Note that the single chip conversion controller 122 or the so-called “bridge circuit” is provided on the motherboard of the storage device 12.

Fig. 2 of the instant Application:



Note that the so-called “bridge circuit” (single chip) 100 is provided on a separate “secondary” board 25, instead of on the motherboard 20 of the storage device.

However, it is clear that whether the single chip conversion controller 122 or the so-called "bridge circuit" is provided on the motherboard of the storage device as in Kobayashi, or provided on a separate or "secondary" board as in claim 5, the conversion controller 122 would perform the same function, which is a function of converting between the ATA/ATAPI protocol to the USB protocol and vice versa. As matter of fact, as disclosed in Applicants' summary of the Invention, the crux of Applicants' claimed invention is a single bridging chip for converting ATA/ATAPI protocol to USB protocol and vice versa. The bridging circuit/chip 100 would perform the same function whether the bridging chip 100 is provided on a motherboard of the storage device (page 2, lines 8-12 of the originally filed specification, and Fig. 3):

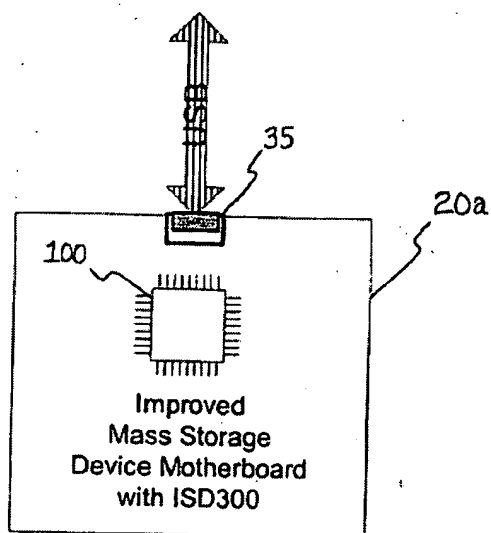


FIG. 3

or, alternatively, as a design choice, the bridging chip 100 is provided on a secondary board (see page 2, lines 17-21 of the originally filed specification, and Fig. 2)

:

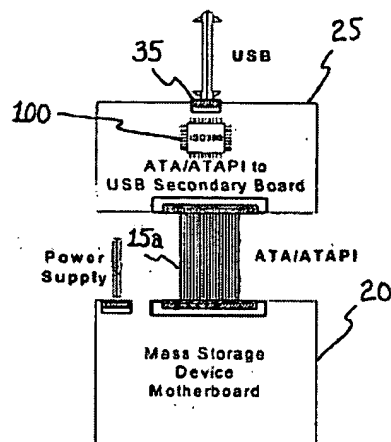
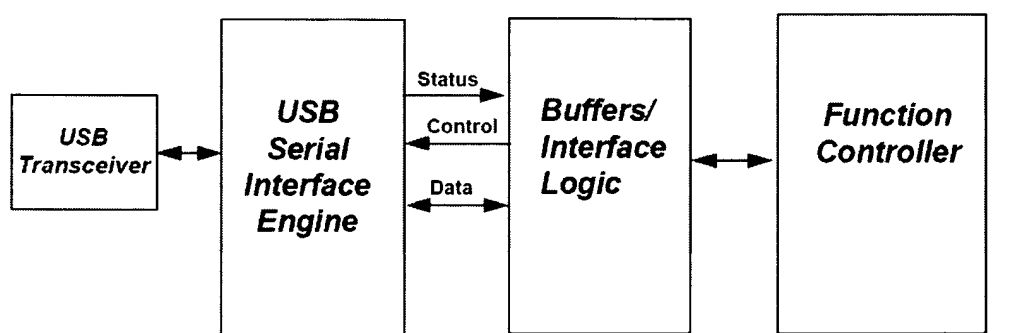


FIG. 2

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a separate or "secondary" board for the single chip conversion controller 122 of Kobayashi, since the conversion controller chip 122 of Kobayashi would perform the same function whether on the same board with the storage device 12 or on a separate or "secondary board" and, thus, providing a separate or "secondary board" for the single chip conversion controller 122 of Kobayashi is a matter of design choice, as also acknowledged by Applicants, and only involves ordinary skill in the art. With regard to claim 9, note that it is clear that it is clearly inherent that the separate or "secondary" board must include a "connector port" for receiving signals from the mass storage device motherboard, and a USB "connector

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port" for outputting USB signals to the so-called "host motherboard" or the motherboard of the computer of Kobayashi. With regard to claims 11 and 12, note also that it is clear from discussion above that the single chip conversion controller 122 is used to convert ATA/ATAPI signals to USB signals and vice versa. Thus, it is clear that the single chip conversion controller 122 includes an ATA/ATAPI interface to take the ATA/ATAPI signal and convert it to a USB signal, a disk interface (any ATA standard provides disk interface) and also a USB interface. Further, since the single chip conversion controller 122 also employs USB protocol for sending USB signals to computer 111 having a USB interface, it must be in full compliance with the USB specification, which requires a serial interface engine; and a USB physical interface transceiver configured to receive signals from the serial interface engine and output USB signals to a USB interface. The following is a diagram of a USB hardware interface according to the USB specification. See designing a robust USB Serial Interface Engine, cited below.



Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi, as applied to claims 9-11 above, and further in view of USB 2.0 Specification.

The further difference between the claimed subject matter and that of Kobayashi resides in the function of the conversion controller 122 or the so-called "bridge circuit" to convert ATA/ATAPI protocol into USB 2.0 protocol. Note that Kobayashi discloses that the conversion controller 122 converts ATA/ATAPI protocol into USB protocol. Note also that Kobayashi does not particularly disclose which version of the USB protocol the term "USB" refers to).

However, USB 2.0 is only an extended version of USB protocol but designed for higher speed communication. See Universal Serial Bus Specification, Revision 2.0, cited below.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ USB 2.0 protocol in the conversion controller 122 of Kobayashi to convert ATA/ATAPI protocol to USB 2.0 protocol, as taught by the disclosure of USB 2.0 specification, for the purpose of providing a higher communication speed to the system of Kobayashi, instead of using lower speed afforded by the USB protocol.

USB in a Nutshell, Designing a Robust USB Serial Interface Engine (SIE), and definition of ATA from Wikipedia are cited as relevant art.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Dang whose telephone number is 571-272-3626. The examiner can normally be reached on Monday to Friday from 9:AM to 5:PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart, can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Khanh Dang
Primary Examiner